

**Triacs
sensitive gate**

BT139B series E

GENERAL DESCRIPTION

Passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

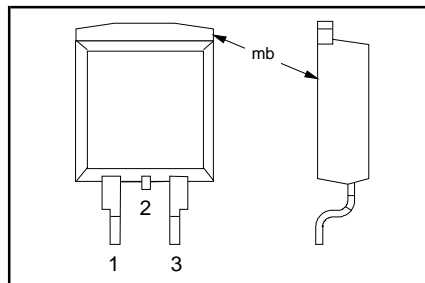
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.		UNIT
		600E	800E	
V_{DRM}	Repetitive peak off-state voltages	600	800	V
$I_{T(RMS)}$	RMS on-state current	16	16	A
I_{TSM}	Non-repetitive peak on-state current	140	140	A

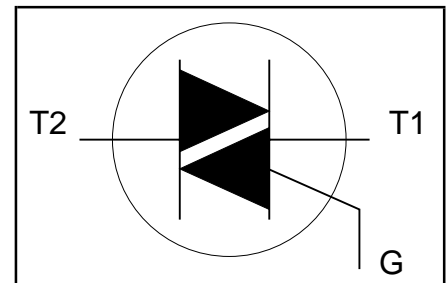
PINNING - SOT404

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
mb	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-600 600 ¹	-800 800	
V_{DRM}	Repetitive peak off-state voltages		-	-600 600 ¹	-800 800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 99\text{ }^\circ\text{C}$	-	16		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25\text{ }^\circ\text{C}$ prior to surge	-	140		A
I^2t	I^2t for fusing	$t = 20\text{ ms}$	-	150		A
di_T/dt	Repetitive rate of rise of on-state current after triggering	$t = 16.7\text{ ms}$	-	98		A ² s
		$t = 10\text{ ms}$	-	10		A μ s
		$I_{TM} = 20\text{ A}; I_G = 0.2\text{ A}; di_G/dt = 0.2\text{ A}/\mu\text{s}$	-	2		A
I_{GM}	Peak gate current	T2+ G+	-	50		A/ μ s
V_{GM}	Peak gate voltage	T2+ G-	-	50		A/ μ s
P_{GM}	Peak gate power	T2- G-	-	50		A/ μ s
$P_{G(AV)}$	Average gate power	T2- G+	-	10		A/ μ s
T_{stg}	Storage temperature		-	2		A
T_j	Operating junction temperature		-	5		V
		over any 20 ms period	-	5		W
			-40	0.5		W
			-	150		$^\circ\text{C}$
			-	125		$^\circ\text{C}$

¹ Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/ μ s.

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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	full cycle	-	-	1.2	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	half cycle minimum footprint, FR4 board	-	-	1.7	K/W
			-	55	-	K/W

STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$				
		T2+ G+	-	3.2	30	mA
		T2+ G-	-	16	40	mA
		T2- G-	-	4.0	30	mA
		T2- G+	-	5.5	40	mA
I_H	Holding current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	4.0	30	mA
V_T	On-state voltage	$I_T = 20\text{ A}$	-	1.2	1.6	V
V_{GT}	Gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.7	1.5	V
I_D	Off-state leakage current	$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 125\text{ °C}$	0.25	0.4	-	V
		$V_D = V_{DRM(max)}; T_j = 125\text{ °C}$	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125\text{ °C};$ exponential waveform; gate open circuit	-	50	-	V/ μ s
t_{gt}	Gate controlled turn-on time	$I_{TM} = 20\text{ A}; V_D = V_{DRM(max)}; I_G = 0.1\text{ A};$ $dI_G/dt = 5\text{ A}/\mu$ s	-	2	-	μ s

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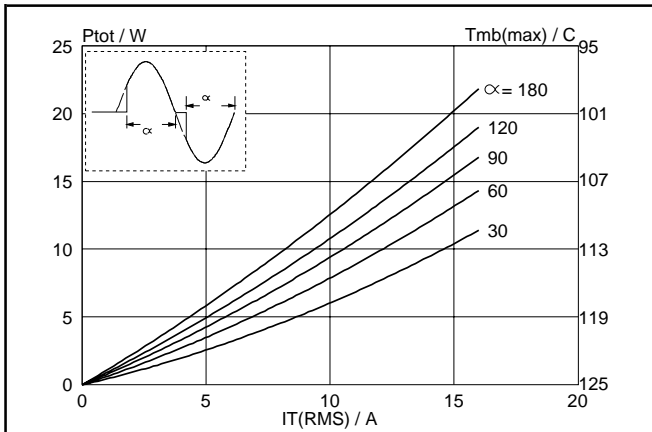


Fig. 1. Maximum on-state dissipation, P_{tot} , versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

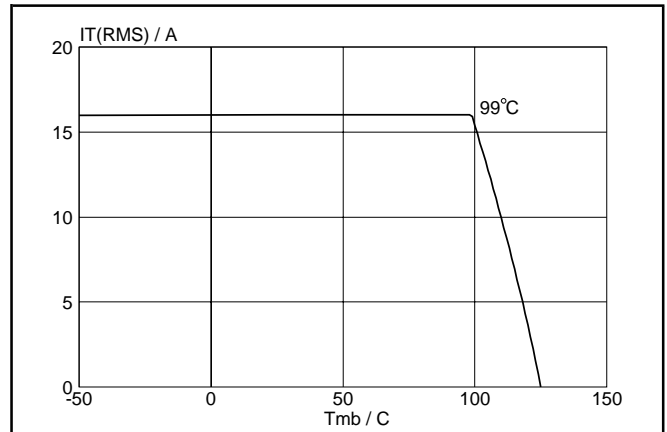


Fig. 4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb} .

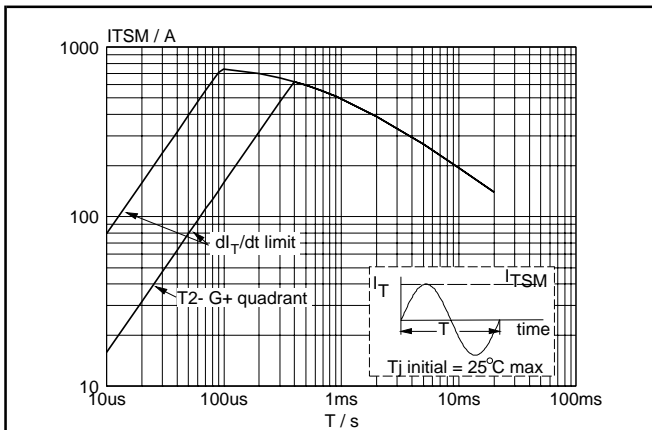


Fig. 2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 20ms$.

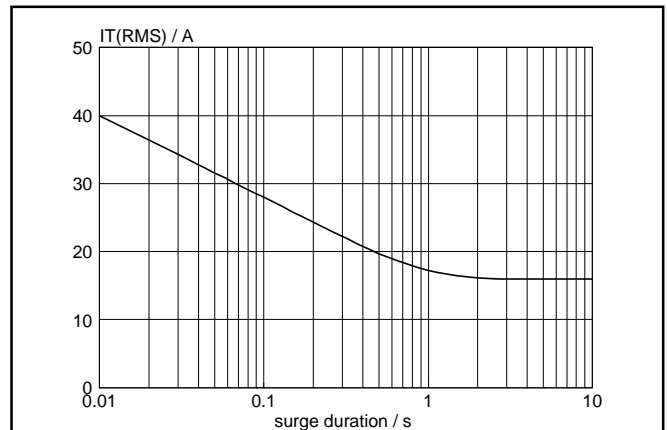


Fig. 5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50 Hz$; $T_{mb} \leq 99^\circ C$.

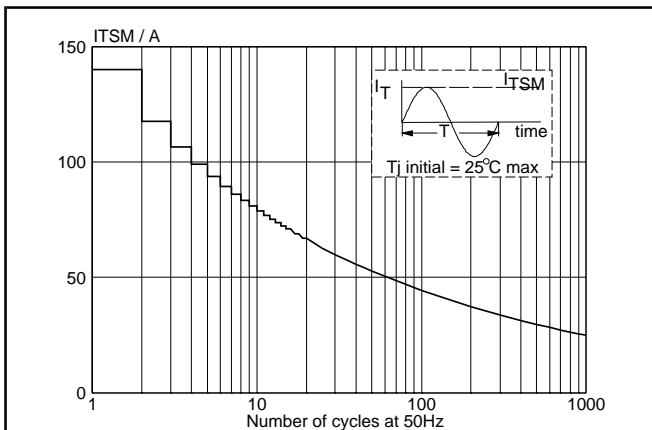


Fig. 3. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50 Hz$.

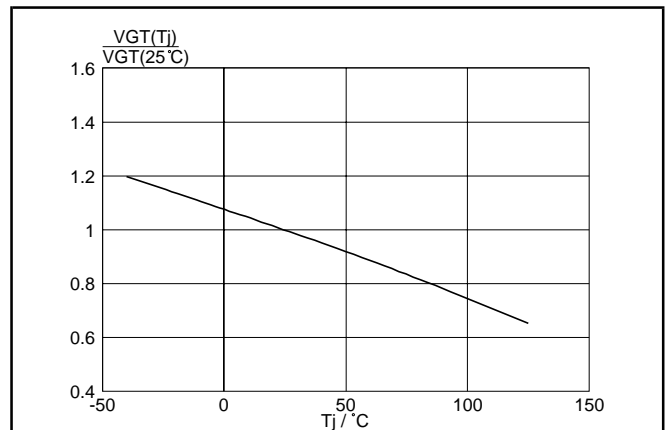
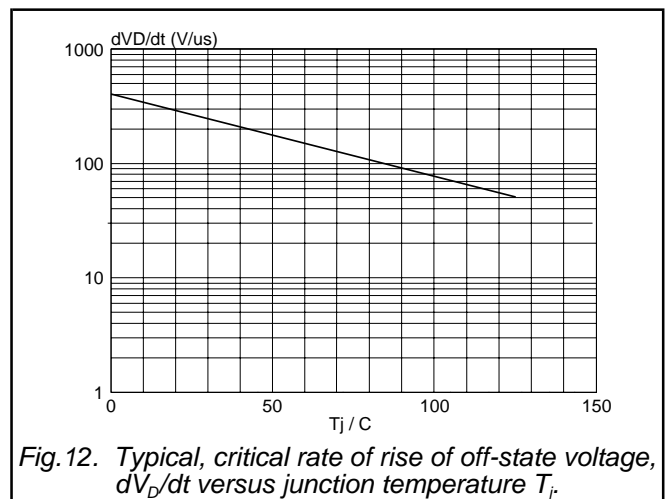
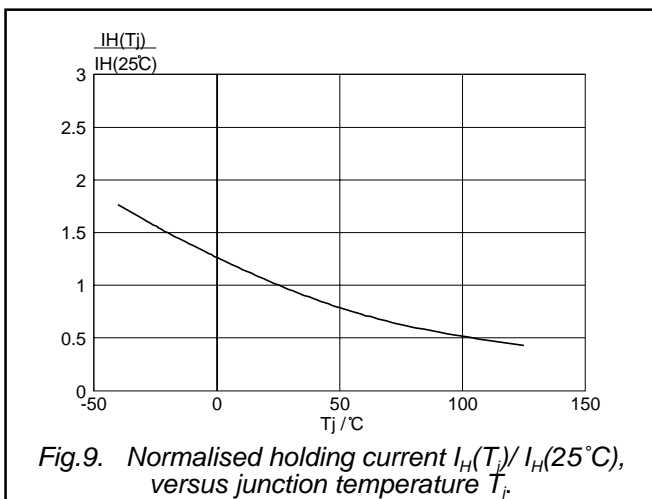
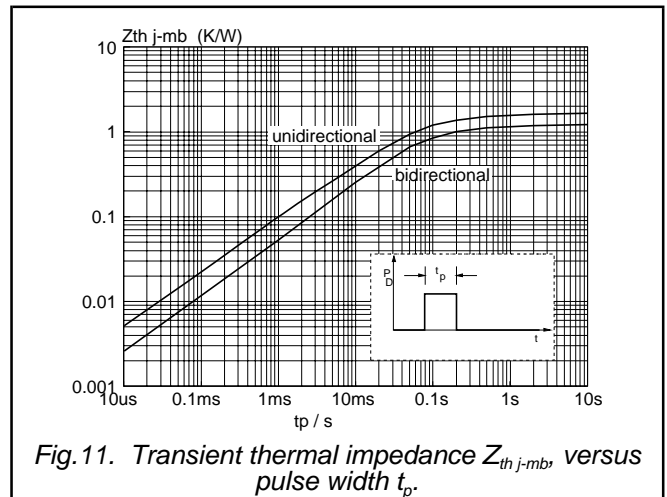
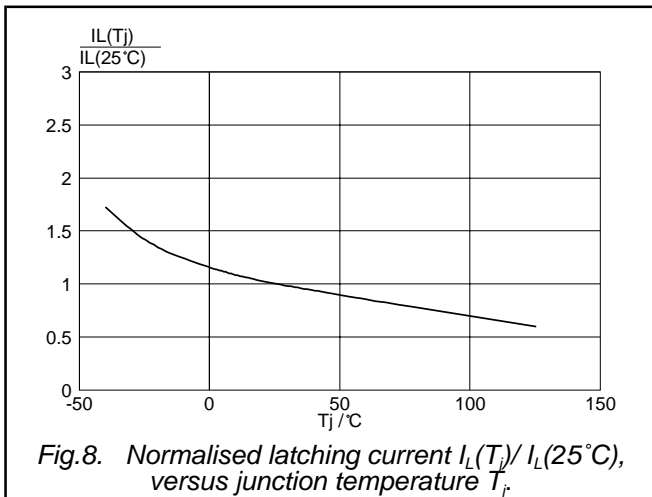
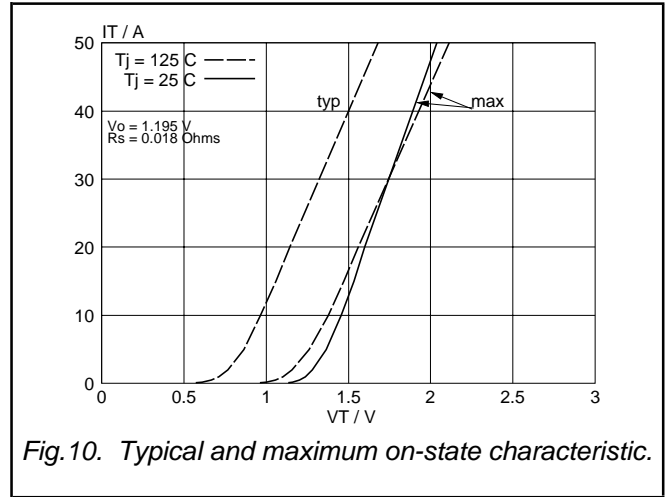
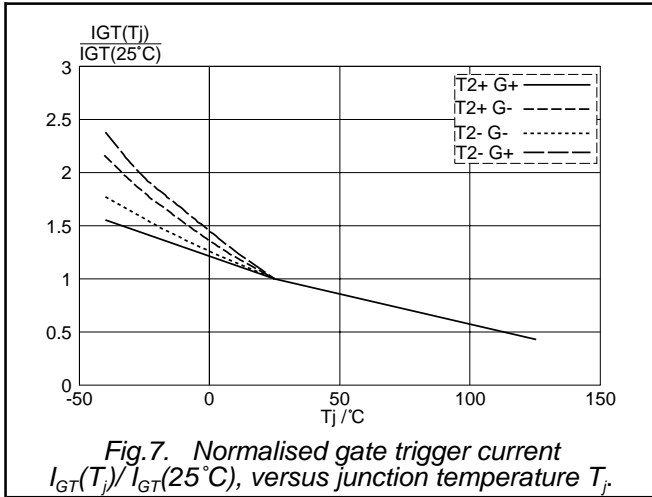


Fig. 6. Normalised gate trigger voltage $V_{GT}(T_j) / V_{GT}(25^\circ C)$, versus junction temperature T_j .

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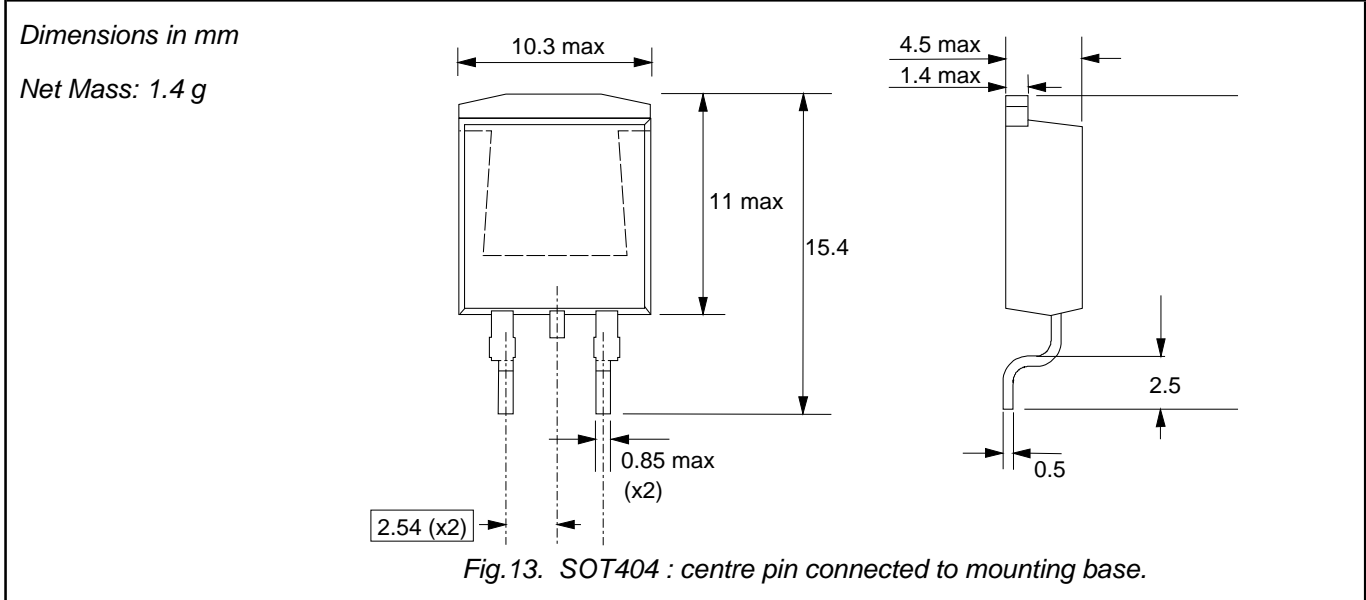
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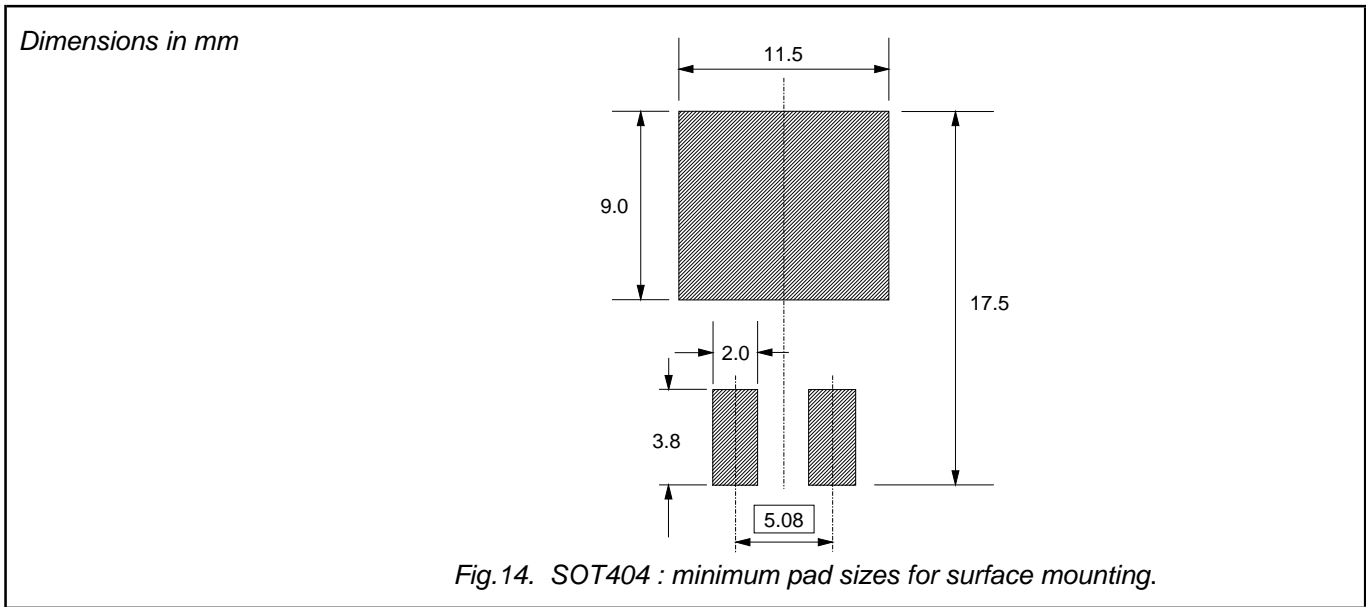
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MECHANICAL DATA



MOUNTING INSTRUCTIONS



Notes

- 1. Plastic meets UL94 V0 at 1/8".

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DEFINITIONS

DATA SHEET STATUS		
DATA SHEET STATUS²	PRODUCT STATUS³	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A
Limiting values		
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		
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² Please consult the most recently issued datasheet before initiating or completing a design.

³ The product status of the device(s) described in this datasheet may have changed since this datasheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.